REMARKS

In the July 10, 2006 office action which was made final, the examiner used the same references that were previously used by him in the prior office action, namely Brewer et al and Dockser.

Although the examiner went into considerable detail in the Final office action attempting to explain that applicants' description of the present invention does not contain explicit language in excluding 'exception' packets, applicants continue to emphasize that this is a major distinction between the invention as claimed and the teachings of Brewer et al. Applicants repeatedly mentioned that their invention provides a means of maintaining the input/output sequence in deep-packet processing tasks. For example:

Page 2, line 8, states "The present invention provides a means of preserving the sequence in deep-packet processing operations in a multiprocessor system."

Page 3, lines 1-4, states "The invention also relates to a multiprocessing system and its method of operation wherein the system includes means for preserving the sequence in which multiple data frames are transmitted to processing functions and the processed frames are forwarded to their destination."

Page 3, lines 14-17, states "The invention also relates to a system and method for transmitting multiple data frames to processing functions in a given sequence, performing the processing on the frames, and forwarding the processed frames to their destination in the same given sequence."

Clearly, if applicants contemplated the handling of "exception" packets, this above-quoted language certainly is counter-suggestive of that intention. The ordering of

the frames in a given sequence is described commencing at line 18 of page 5 of the present invention which states "To avoid losing frames, the Frame Header Processing Unit (**18** in Figure 1) must be able to meet the frame arrival rate. The arbitration/sequencing unit **22** assigns an ascending 'frame sequence number' (FSN) to each frame **12** as it gets assigned to a core engine **20**. The FSN is used to order the frames for transmission. In other words, frames are assigned frame sequence numbers 0, 1, 2 and so forth. The FSN is increasing modulo K, where K is greater or equal to the maximum number of frames that can be in the system at any given time. The core engines operate on frames independently of one another. Once a core engine **20** has completed its processing of a frame **12**, the engine returns the frame to the arbitration/sequencing unit **22**. This unit **22** in turn places the frame in the I/O DMU send frame side buffer **30** for transmission. The frames are buffered and transmitted on the DMU send side according to their assigned FSNs in the ascending order. Thus, a frame with FSN = j+1 cannot be sent unless and until the frame with FSN = j has been sent or has been corrupted."

By this amendment to the claims, applicants have focused all attention on claims 21 and 22, and have canceled all of the other claims. These two remaining independent claims confirm that the input and the output buffers both are contained in a Data Moving Unit. They also unequivocally specify that the frames are forwarded to their destinations in the same sequence in which they are received for processing. Respectfully, applicants submit that this feature is absent in the prior art teachings cited and applied by the examiner.

Element or step c) of each of the two claims has been amended to clearly show that the search engines are assigned the frames in accordance with the type of processing that is to be conducted on the frame. This feature is described in the second full paragraph on page 7 of applicants' specification.

Furthermore, it should be noted specifically that element f) of claim 21 and step f) of claim 22 clearly spell out that the frames from the output buffer are sequenced in the same order as they are received in the input buffer. Therefore, the examiner's contention that this sequencing carries no weight because it appears only in the preamble of these two claims cannot be supported and should be withdrawn. Because this feature serves to distinguish over the prior art and is not rendered obvious by the respective or combined teachings of Brewer et al and Dockser, these two claims should be considered to be in condition for immediate allowance.

This amendment substantially reduces the number of claims in the application, thereby simplifying and minimizing the scope of the review of this amendment by the examiner, and the issues in the event of an appeal. Accordingly, entry of this amendment after final is respectfully requested.

Brewer et al relate solely to maintaining router packet control. The reference does not perform any service in the packets or frames such as encryption or compression. The filtering function discussed in this reference is performed solely on the frame header, and does not constitute substantive deep pocket processing on the frame. It merely determines from the header whether the frame destination is local or external. As covered on page 1 of the present application, this activity is superficial and does not constitute 'deep-packet processing' by going beyond the header into the data itself.

Furthermore, it should be noted that the packet forwarding engine of Brewer et al is equivalent to the Frame Header Processing Unit of applicants' invention. It inspects the frame header but does not do any deep processing on the data in the frame. The examiner's interpretation of the filtering function of the reference as a deep packet process is, respectfully, categorically incorrect. Applicants have now amended the two remaining claims to indicate that the processing done by the core engines is performed on the frame data, and not the header. This further distinguishes the invention over the teachings of the references.

Yet an additional distinction resides in the claim limitation that the core engines include an associated memory for storing a frame assigned to the engine until it can be processed. Brewer et al do not appear to contain such a limitation.

Although the examiner has combined the teachings of Brewer with the teachings of Dockser to show that larger buffer size has an advantage over a smaller size, it should be pointed out that the combined teachings of these two references does not suggest that the input and the output buffer are contained within a singular Data Moving Unit. This limitation is included in claims 21 and 22, and serves to further distinguish applicants' claimed invention over the applied prior art.

CONCLUSION

Applicants respectfully submit that the amendment to the claims now places the application in condition for immediate allowance. Accordingly, amended claims 21 and 22, the only two remaining in the application, should, therefore, be deemed to be allowable. The examiner is respectfully requested to take such action as is consistent therewith.

If there are any minor matters that can easily be resolved by phone or by email, the examiner is encouraged to contact the undersigned as a step toward resolution.

Reconsideration and allowance are now respectfully requested.

Respectfully submitted,

Date: SEPTEMBER 11, 2006

James A. Lucas, Reg. No. 21,081
CUSTOMER NUMBER 26675